CLAIMS

1. (currently amended) A method for filling a line in a cache, comprising the steps of:

sending a request for data to be provided on a data bus to the cache at a first address;

sending a first request external to the cache for first data at the first address;

defining a first pointer for the first address;

sending for additional data at additional addresses, the additional addresses being consecutive with the first address;

defining a second pointer for the address of the data that was last sent for;

receiving the first data located at the first address;

placing the first data in the line in the cache and onto the data bus;

loading the additional data into the line in the cache as it is received without waiting for completion of the step of placing the first data in the line in the cache and onto the data bus;

defining a third pointer for the address of the data that was last received;

terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses; and

sending the second request external to the cache for the different data at the different address.

2. (original) The method of claim 1, further comprising:

continuing loading the additional data into the line in the cache as it is received in response to receiving a data request at one of the additional addresses for data not present in the cache.

3.-9. (canceled)

10. (currently amended) A processing system comprising:

a cache for storing data and providing a hit signal if a request for data is contained in the cache and a miss signal if the request for data is not contained in the cache;

processor means, coupled to the cache, for sending a request for data to the cache at a first address;

fetch means, coupled to the cache and the processor means, for sending the request external to the cache for first data at a first address in response to the miss signal, sending for additional data at additional addresses, the additional addresses being consecutive with the first address, receiving the first data located at the first address, placing the first data in the cache and onto the data bus, loading the additional data into the line as it is received without waiting for completion of the loading of the additional data into the line as it is received, tracking progress of the requests for the data at the additional addresses by setting a first pointer for the first address, a second pointer for the address of the additional addresses that was last sent out, and a third pointer for the address of the additional addresses of the additional data that was last loaded, and terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses.

B1

11. (original) The processing system of claim 10, wherein the fetch means is further characterized as sending the second request external to the cache for the different data at the different address.

12. (previously amended) The processing system of claim 11, wherein the cache is characterized as having plurality of lines that each comprise locations having consecutive addresses, and wherein the additional addresses requested by the fetch means are for locations in the cache that are in a line in the plurality of lines.

13. (original) The processing system of claim 12, further comprising a system interface coupled to the fetch for interfacing between the fetch means and an external memory.

14. (original) The processing unit of claim 10 wherein the fetch means is further characterized as continuing loading the additional data if a third request is received from the processor means that is a miss in the cache and is for one of the additional addresses.